In the Specification:

On page 1, line 3, immediately above "Background of the Invention", please insert the following paragraph:

The present application is a continuation of U.S. patent application serial number 09/312,064, filed May 13, 1999.

On page 10, please amend Table 1 as follows:

Table 1. PDC High-speed Phone Side Data Mode Connector

Name of Pin	PDC High Speed Data Mode Signal Description	Direction
TCH_TX	Transmit synchronous data (28 Bytes / frame)	PDC←PC
TCH_FRAME	This signal tells if the current frame is Rx (H) or Tx (L).	PDC→PC
TCH_CLOCK	Clock signal (42kbps bit rate intermittent clock)	PDC→PC
~~Cell~~CTL_TX	TX control serial data (600 – 9600 bps)	PDC←PC
~~Cell~~CTL_RX	RX control serial data (600 – 9600 bps)	PDC→PC
TCH_RX	Receive synchronous data (28 Bytes / frame)	PDC→PC
ADP	Indication whether PC is connected to PDC	PDC←PC
PDC Control signal1	Signal to enable the direct memory access of the PDC phone for Phone book support	PDC←PC

On page 11, please amend Table 2 as follows:

Table 2. PDC Packet Mode Connector

Name of Pin	PDC High-speed Data Mode Signal Description	Direction
TCH_TX	Transmit synchronous data (HDLC frame)	PDC←PC
TCH_FRAME	This signal tells if the system is in communication	PDC→PC
TCH_CLOCK	Clock signal (42kbps LAPB clock)	PDC→PC
~~Cell~~CTL_TX	TX control serial data (600 – 9600 bps)	PDC←PC
~~Cell~~CTL _RX	RX control serial data (600 – 9600 bps)	PDC→PC
TCH_RX	Receive synchronous data (HDLC frame)	PDC→PC
ADP	Indication whether PC is connected to PDC	PDC←PC
PDC Control signal1	Signal to enable the direct memory access of the PDC phone for Phone book support	PDC←PC

Please amend paragraph starting on page 13, line 25 through page 14, line 7, as follows:

FIG. 6 is a block diagram depicting additional details of the data path from the TCH RxTx 62 to the Endpoint-1 block [44] 46. The TCH RxTx 62 sends data 108 to the FIFO ~~50~~ 52. The FIFO write control module 102 is used to set the proper address in the FIFO 50 to store the data 108. The TCH TxRx 62 is also connected to the Frame Sync Logic module 54. The Frame Sync Logic module 54 is used to mark the beginning of each data frame. As indicated, the beginning of each frame is marked with a "1" in the first bit position 107. The Frame Sync Logic module 54 is also connected to the FIFO read control module 101. The FIFO read control module 101 controls the Multiplexer (MUX) 100 for controlling the selection and transmission of data from the FIFO 50 to Endpoint-1 44. As indicated, in this example, a bulk transfer of 8

bytes is sent to the Endpoint-1 44 upon each data transfer. In accordance with standard USB protocol, this can occur at a maximum rate of once every millisecond.

Please amend paragraph on page 14, lines 8-16, as follows:

FIG. 7 is a block diagram depicting additional details of the data path from the Endpoint-1 44 to the TCH RxTx 62. Endpoint-1 44 sends data to the Receive FIFO ~~52~~ 50. This transfer is controlled by the FIFO write control module 121, which sets the proper FIFO address so that data is stored in the proper location and in the proper order. The Frame Sync Logic module 54 is used to mark the beginning of each data frame by setting a "1" in the mark (i.e. first) bit position 124 to indicated the beginning of the frame, and by setting a "0" in the bit position 124 for all other data bytes. The TCH RxTx module 62 is also coupled with the Frame Sync Logic module 54 as shown. This connection enables the FIFO read control 122 to control the MUX 125 for sending data from the FIFO ~~52~~ 50 to the TCH RxTx 62 when the TCH_FRAME signal is low.

Please amend paragraph on page 28, lines 20-24, as follows:

FIG. 10 is a block diagram depicting additional details of the wireless protocol stack 171 that can be used in the PDC protocol implementation described in the example embodiments herein. As shown, the application program 150 interfaces with the ~~CCB~~ CCS 183. In this example, the ~~CCB~~ CCS 183 comprises the same components as the previous example, namely the AT parser 180, the call control module 182, the V.42bis protocol stack 184 and the plug-in modules 181.

Please amend paragraph on page 28, lines 25-26, as follows:

The ~~CCB~~ CCS 183 is coupled to the hardware access driver HAD 154. As shown, the HAD is coupled to the USB controller 11, which is coupled with the MPI 16.

Please amend paragraph starting on page 28, line 27 through page 29, line 4, as follows:

Details of the external PIM 174 are shown in FIG, 10. In particular, the external PIM comprises an initialize and terminate module ~~192~~ 193 and a protocol stack 171. The protocol stack 171 comprises the following components. As stated, the PDC protocol comprises a data channel and a control channel. In this example, the three modules 185, 186 and ~~186~~ 187 are used to implement the control channel. Similarly, the three modules 188, 189, and 190 are used to implement the data channel.

Please amend paragraph on page 30, lines 7-10, as follows:

FIG. 11 is a block diagram depicting additional details of the ~~the~~ data flow between the ~~MPC~~ MPI 16 and the application program (also referred to as DTE) 150. In the figure below, storage locations that are queues end with a "Q" or a "queue" designation. Buffer storage devices are referred to with a "Buffer" designation as part of the name.